CLAIM AMENDMENTS

1. (Currently amended) An apparatus, comprising:

a wafer portion that comprises a conduction layer;

wherein upon exposure of the conduction layer during an etch of the wafer portion, the conduction layer serves to dissipate a portion of a charge buildup on the wafer portion, and wherein the conduction layer is electrically coupled with a silicon layer of the wafer portion; and

wherein removal of a portion of the silicon layer from the wafer portion during the etch serves to expose the conduction layer.

2. (Canceled)

3. (Currently amended) The apparatus of claim 1 [[2]], ~~wherein the conduction layer is electrically coupled with the silicon layer of the wafer portion;~~

wherein the etch serves to create one or more sidewalls in a portion of the silicon layer, and wherein the conduction layer is electrically coupled with the one or more sidewalls; and

wherein the one or more sidewalls and the conduction layer serve to dissipate the portion of the charge buildup on the wafer portion.

4. (Original) The apparatus of claim 3, wherein the one or more sidewalls comprise one or more electrostatic potentials substantially similar to an electrostatic potential of the conduction layer;

wherein the one or more electrostatic potentials of the one or more sidewalls serve to dissipate the portion of the charge buildup from the one or more sidewalls.

5. (Currently amended) The apparatus of claim 1, ~~wherein the conduction layer is electrically coupled with a silicon layer of the wafer portion,~~ wherein the wafer portion comprises a backing layer coupled with the conduction layer; and

wherein the backing layer provides structural integrity to the wafer portion; and

wherein the backing layer insulates the conduction layer.

6. (Original) The apparatus of claim 5, wherein the backing layer comprises a photoresist.

7. (Original) The apparatus of claim 1, wherein the conduction layer serves to mitigate one or more etch rate variations across the wafer portion.

8. (Original) The apparatus of claim 1, wherein the conduction layer neutralizes the portion of the charge buildup on the wafer portion.

9. (Original) The apparatus of claim 1, wherein the conduction layer comprises a conductive material.

10. (Original) The apparatus of claim 9, wherein the conductive material comprises aluminum.

11. (Original) The apparatus of claim 1, wherein the conduction layer comprises a thickness in the range of about one half micrometer ("μm") to about two micrometers.

12. (New) The apparatus of claim 1, wherein said etch is selected from the group consisting of a Deep Reactive Ion Etch (DRIE) and a Bosch process.